



#13  
mm  
4-28-01 AF  
GP2700

RECEIVED

§ Group Art Unit: 2161  
§  
§ Examiner: Elisca, P.  
§  
§ Atty. Dkt. No.: 5181-15900

APR 23 2001

Technology Center 2100

Serial No.: 09/097,468

Filed: June 15, 1998

For: TESTING DEVICE DRIVER  
HARDENING

CERTIFICATE OF MAILING  
37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below:

B. Noel Kivlin  
Name of Registered Representative

April 16, 2001  
Date

Signature \_\_\_\_\_

# APPEAL BRIEF

Box AF  
06/06/2003 MJONES1: 00000001 501505 09097468  
Assistant Commissioner for Patents  
01 FC:1401 380-00-54  
Washington D.C. 20231

Sir/Madam:

Further to the Notice of Appeal filed February 14, 2001, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

**I. REAL PARTY IN INTEREST**

The subject application is owned by Sun Microsystems, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at 901 San Antonio Road, Palo Alto, California 94303.

RECEIVED

APR 23 2001

Technology Center 2100

**II. RELATED APPEALS AND INTERFERENCES**

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

**III. STATUS OF CLAIMS**

Claims 1-26 are pending and stand finally rejected under 35 U.S.C. §103(a) and are the subject of this appeal. A copy of claims, as on appeal (incorporating all amendments), is included in the Appendix hereto.

**IV. STATUS OF AMENDMENTS**

No amendments have been filed since subsequent to the final rejection, which was issued on November 2000.

**V. SUMMARY OF THE INVENTION**

Appellant's claimed invention relates to the testing of device driver hardening. A test mechanism for testing device driver hardening comprises an intercept mechanism for intercepting device access calls from a device driver under test and an interface for

configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined test pattern.

Accordingly an embodiment of the invention provides a hardened driver test mechanism. This test mechanism provides a harness enabling the arbitrary introduction of typical faults. These faults may be introduced totally asynchronously and to emulate real life.

The intercept mechanism can comprise a test module which can be loaded into the operating system. Once loaded the test module can intercept all of the device access calls. It mimics the normal functions of these calls accessing the offset address and propagating the appropriate data. This test module can comprise a test driver and a plurality of intercept routines. The interface can be in the form of a programming interface (API) which allows user test applications to supply information to the driver for configuring the intercept routines to provide specific corruption of data obtained through device accesses.

The device access calls are redirected/mapped to the intercept routines by a device access infrastructure. This redirecting/mapping could be achieved using a lookup table. Alternatively other redirecting/mapping mechanisms could be used.

The device access infrastructure of a device driver interface mechanism can be responsive to a device driver interface access request to intercept the request for the selective insertion of errors, whereby the subsequent device driver access call causes device access with the performing of an additional pre-specified logical/arithmetical operation on the data so obtained or does not cause device access, but instead the return of an emulated device response.

An embodiment of the invention overcomes the problem that it is not normally possible to have sufficient access to the hardware design of a device to be able to inject a

suitable varied range of faults. Modern device drivers access hardware through a set of specific functions. The use of these functions within a compliant driver can facilitate the construction of a hardened driver test mechanism.

The present test mechanism allows a test engineer to specify a reference to (for example) a specific device, a specific register set on that device, an offset range, a data mask value, a logical/arithmetic operator (=, NOT, AND, OR, XOR, +, -) and an access count. Intercept routines then check each use by the device driver interface of the device access calls to see if it is within the specified parameters. A count is decremented on each matching occurrence. When the count has expired the data read can be operated upon by a pre-specified operator and operand. This allows a test mechanism to introduce a vast range of different faults. In accordance with another aspect of the invention, there is provided a computer program product on a carrier medium, the computer program product comprising a test mechanism as described above.

In accordance with a further aspect of the invention, there is provided a test application on a carrier medium for a test mechanism as described above. The test application comprises computer code configured to be operable to provide the test mechanism with a test configuration, to detect the response of a driver to a test condition inserted by the test mechanism, to compare the detected response to an expected response set out in a test script and to identify discrepancies between the detected response and the expected response. The test application can also be operable to maintain a log of the detected responses.

In accordance with a further aspect of the invention, there is provided a computer comprising a processor, memory, an I/O bus controller, at least one I/O device, a device driver for accessing the I/O device, and a test mechanism as described above.

In accordance with a further aspect of the invention, there is provided a method of testing the hardening of a device driver, the method comprising intercepting device

access calls initiated from the device driver and redirecting them via a test module comprising at least one intercept routine for injecting a fault in a response to the device access function call according to a desired test pattern.

## **VI. ISSUES**

Whether claims 1-26 are patentable under 35 U.S.C. § 103(a) over Tavallaei et al. (U.S. Patent No. 5,864,653) in view of Splett et al. (U.S. Patent No. 5,001,712).

## **VII. GROUPING OF CLAIMS**

Claims 1-2 stand or fall together.

Claim 3 stands or falls alone.

Claim 4 stands or falls alone.

Claim 5 stands or falls alone.

Claim 6 stands or falls alone.

Claims 7-8 stand or fall together.

Claim 9 stands or falls alone.

Claim 10 stands or falls alone.

Claim 11 stands or falls alone.

Claim 12 stands or falls alone.

Claim 13 stands or falls alone.

Claim 14 stands or falls alone.

Claims 15-16 stand or fall together.

Claim 17 stands or falls alone.

Claim 18 stands or falls alone.

Claim 19 stands or falls alone.

Claim 20 stands or falls alone.

Claim 21 stands or falls alone.

Claim 22 stands or falls alone.

Claim 23 stands or falls alone.

Claims 24-26 stand or fall together.

The reasons why each group of claims is believed to be separately patentable are explained below in the Argument.

## VIII. ARGUMENT

### A. Claims 1-2

Claims 1-2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. (U.S. Patent No. 5,864,653) in view of Splett et al. (U.S. Patent No. 5,001,712). The Examiner's position is that the references, taken in combination, teach all of the elements of claims 1-2. Appellant asserts that this rejection is erroneous for the following reasons.

The Examiner states that "Tavallaei substantially discloses a PCI hot spare capability for failed components and a SMC for running boundary scan test on the system **which is equivalent to the test mechanism for testing device drivers(sic)**" (Emphasis added). Appellant submits that this statement is erroneous. As defined in *The New IEEE Standard Dictionary of Electrical and Electronics Terms*, Fifth Edition, a device driver is "the software that translates device-independent commands into device-specific commands". Device drivers are thus software entities. In contrast, boundary scan test is directed to the testing of hardware. Appellant therefore asserts that device driver testing and boundary scan testing are not at all equivalent, and in fact, are associated with completely different fields of endeavor.

Appellant submits that neither Tavallaei nor Splett teach or suggest device drivers, and consequently, provide no teaching or suggestion of "a test mechanism comprising an intercept mechanism for intercepting device access calls from **a device**

**driver under test** and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined test pattern” (Emphasis added). Appellant therefore asserts that the references, taken singly or in combination do not teach or suggest all of the elements of claims 1 and claim 2.

In light of the above remarks, Appellant asserts that the rejection of claims 1-2 erroneous.

**B. Claim 3**

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 3 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest an intercept mechanism comprising a plurality of intercept routines “wherein each intercept routine is for a given type of device access call.” Appellant can find no teaching or suggestion of an intercept mechanism as recited in claim 3 in either of the cited references, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 3 is erroneous.

**C. Claim 4**

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 4 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “comprising a mapping mechanism for mapping device access calls to intercept routines.” Appellant can find no teaching or suggestion of a test mechanism as recited in claim 4 in either of the cited references, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 4 is erroneous.

**D. Claim 5**

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 5 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a mapping mechanism “wherein the mapping mechanism comprises a look-up table.” Appellant can find no teaching or suggestion of a mapping mechanism as recited in claim 5 in either of the cited references, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 5 is erroneous.

**E. Claim 6**

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 6 depends from independent claim 1. In

addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism having an intercept mechanism “wherein the intercept mechanism is operable to monitor device access calls to determine when to inject a fault.” Appellant can find no teaching or suggestion of an intercept mechanism as recited in claim 6 in either of the cited references, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 6 is erroneous.

**F. Claims 7 and 8**

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claims 7 and 8 depend from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of these claims is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest “a counter associated with at least one predetermined type of device access call, the intercept mechanism being configured to monitor the counter which is modified for each device access call of that type, and to be operable to inject a fault in response to a determined count of the counter” as recited in claim 7. Furthermore, Appellant submits that neither Tavallaei nor Splett teach or suggest “a second counter for determining a number of times a fault is to be injected for successive device access calls of the predetermined type” as recited in claim 8. It is also noted that neither Tavallaei nor Splett provide any mention of device access calls, and consequently, Appellant asserts that neither of the cited references teach or suggest a counter as recited in claim 7, or a second counter as recited

in claim 8. Appellant therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of these claims.

In light of the above remarks, Appellant asserts that the rejection of claims 7 and 8 are erroneous.

**G. Claim 9**

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 9 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein each type of device call is separately monitored.” Appellant can find no teaching or suggestion of a test mechanism as recited in claim 9 in either of the cited references, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 9 is erroneous.

**H. Claim 10**

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 10 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein a device access infrastructure is responsive to a device access call to intercept the call for the selective insertion of faults and the intercept mechanism is

operative to return an emulated device response.” Appellant can find no teaching or suggestion in either of the cited references of a test mechanism as recited in claim 10 and therefore submits that the cited references, taken singly or in combination, do not teach all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 10 is erroneous.

**I. Claim 11**

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 11 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein a device access infrastructure is responsive to a device access call to intercept the call and the intercept mechanism is operable to provide selective insertion of faults prior to effecting the device access.” Appellant can find no teaching or suggestion in either of the cited references of a test mechanism as recited in claim 11 and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 11 is erroneous.

**J. Claim 12**

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 12 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein the intercept mechanism operates on data of a device access call with a determined operator and operand.” Appellant can find no teaching or suggestion in either of the cited references of a test mechanism as recited in claim 12 and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 12 is erroneous.

**K. Claim 13**

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 13 depends from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein the interface is operable to configure the intercept mechanism for determining when the intercept mechanism injects a fault.” Appellant can find no teaching or suggestion in either of the cited references of a test mechanism as recited in claim 13 and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 13 is erroneous.

**L. Claim 14**

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 14 depends from independent claim 1. In

addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a test mechanism “wherein the interface comprises an application program interface responsive to a test application for determining a test pattern.” Appellant can find no teaching or suggestion in either of the cited references of a test mechanism as recited in claim 14 and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 14 is erroneous.

**M. Claims 15 and 16**

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claims 15 and 16 depend from independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of these claims is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest computer code configured to be operable “to detect the response of a device driver to a test condition” and “to compare the detected response to an expected response set out in a test script” as recited in claim 15.

Appellant further submits that neither Tavallaei nor Splett teach or suggest a test application “wherein the test application comprises computer code configured to be operable to maintain a log of the detected responses” as recited in claim 16.

Appellant therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of these claims.

In light of the above remarks, Appellant asserts that the rejection of claims 15 and 16 is erroneous.

**N. Claim 17**

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 17 is an independent claim, and recites a combination of features similar to the combination recited in independent claim 1. In addition to the reasons given above for independent claim 1, Appellant submits that the rejection of independent claim 17 is erroneous for the following additional reasons.

Claim 17 recites “A computer program product on a carrier medium, the computer program product comprising an intercept mechanism for intercepting **device access calls** from a **device driver under test** and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined desired test pattern.” (Emphasis added). Neither Tavallaei nor Splett teach or suggest a computer program product on a carrier medium according to this combination of features, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 17 is erroneous.

**O. Claim 18**

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 18 is an independent claim, and recites a combination of features similar to the combination recited in independent claim 1. In addition to the reasons given above for independent claim 1, Appellant submits that the rejection of independent claim 17 is erroneous for the following additional reasons.

Claim 18 recites “A test mechanism **for testing device driver hardening**, the test mechanism comprising a means for intercepting **device driver access calls** from a **device driver under test** and means for injecting a fault in a response to the device access call according to a determined test pattern.” (Emphasis added). Neither Tavallaei nor Splett teach or suggest a test mechanism according to this combination of features, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 18 is erroneous.

**P. Claim 19**

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 19 is an independent claim, and recites a combination of features similar to the combination recited in independent claim 1. In addition to the reasons given above for independent claim 1, Appellant submits that the rejection of independent claim 19 is erroneous for the following additional reasons.

Claim 19 recites “A computer comprising **a device driver** for accessing an I/O device and **a test mechanism for testing device driver hardening**, the test mechanism comprising an intercept mechanism for intercepting **device access calls** from a **device driver under test** and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined test pattern.” (Emphasis added). Neither Tavallaei nor Splett teach or suggest a computer according to this combination of features. Specifically, neither Tavallaei nor Splett teach or suggest a computer having a test mechanism for testing device driver hardening. Appellant can find no teach or suggestion of the testing of device driver hardening in either Tavallaei or Splett. Appellant therefore submits the cited references, taken singly or in combination, do not teach or suggest all of the limitations of claim 19.

In light of the above remarks, Appellant asserts that the rejection of claim 17 is erroneous.

**Q. Claim 20**

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 20 is an independent claim, and recites a similar combination of features as independent claim 1. In addition to the reasons stated above for claim 1, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Claim 20 recites “a method of **testing the hardening of a device driver**, the method comprising intercepting **device driver access calls** from the **device driver** and injecting a fault in a device driver access according to a desired test pattern.” (Emphasis added). Appellant can find no teaching or suggestion of a method for testing device driver hardening as recited in independent claim 20 in either of the cited references, and therefore asserts that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of claim 20.

In light of the above remarks, Appellant asserts that the rejection of claim 20 is erroneous.

**R. Claim 21**

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 21 depends from independent claim 20. In addition to the reasons stated above for claim 20, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a method “comprising a mapping the device access call to at least one intercept routine for handling the device access call.” Appellant can find no teaching or suggestion in either of the cited

references of a method as recited in claim 21, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 21 is erroneous.

**S. Claim 22**

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 22 depends from independent claim 20. In addition to the reasons stated above for claim 20, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a method “comprising mapping a device access call to an intercept routine according to a device access call type.” Appellant can find no teaching or suggestion in either of the cited references of a method as recited in claim 22, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 22 is erroneous.

**T. Claim 23**

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claim 23 depends from independent claim 20. In addition to the reasons stated above for claim 20, Appellant submits that the rejection of this claim is erroneous for the following additional reasons.

Appellant submits that neither Tavallaei nor Splett teach or suggest a method “comprising monitoring device access call to determine when to inject a fault.” Appellant can find no teaching or suggestion in either of the cited references of a method as recited in claim 23, and therefore submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of this claim.

In light of the above remarks, Appellant asserts that the rejection of claim 23 is erroneous.

**U. Claims 24-26**

Claims 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei et al. in view of Splett et al. Claims 24-26 depend from independent claim 20. In addition to the reasons stated above for claim 20, Appellant submits that the rejection of these claims is erroneous for the following additional reasons.

Claim 24 recites a method “comprising modifying a count for each device access call of a given type and injecting a fault in response to predetermined count being attained.” Claim 25 recites a method “comprising separately monitoring each type of call.” Claim 26 recites a method “comprising a further step of monitoring a number of times the fault is to be injected in sequence.” Appellant submits that neither Tavallaei nor Splett teach or suggest a method according to any of the combinations of features recited in claims 24-26, and further submits that the cited references, taken singly or in combination, do not teach or suggest all of the limitations of these claims.

In light of the above remarks, Appellant asserts that the rejection of claims 24-26 is erroneous.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims was erroneous, and reversal of her decision is respectfully requested.

Respectfully submitted,



B. Noel Kivlin  
Reg. No. 33,929  
Attorney for Appellant

Conley, Rose & Tayon, P.C.  
P.O. Box 398  
Austin, TX 78767-0398  
(512) 703-1271

Date: April 16, 2001

appeal\_brief

## X. APPENDIX

The claims on appeal are as follows.

1. A test mechanism for testing device driver hardening, the test mechanism comprising an intercept mechanism for intercepting device access calls from a device driver under test and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined test pattern.
2. The test mechanism of claim 1, wherein the intercept mechanism comprises a plurality of intercept routines.
3. The test mechanism of claim 2, wherein each intercept routine is for a given type of device access call.
4. The test mechanism of claim 2, comprising a mapping mechanism for mapping device access calls to intercept routines.
5. The test mechanism of claim 4, wherein the mapping mechanism comprises a look-up table.
6. The test mechanism of claim 1, wherein the intercept mechanism is operable to monitor device access calls to determine when to inject a fault.
7. The test mechanism of claim 1, comprising a counter associated with at least one predetermined type of device access call, the intercept mechanism being configured to monitor the counter which is modified for each device access call of that type, and to be operable to inject a fault in response to a determined count of the counter.

8. The test mechanism of claim 7, comprising a second counter for determining a number of times a fault is to be injected for successive device access calls of the predetermined type.

9. The test mechanism of claim 3, wherein each type of device access call is separately monitored.

10. The test mechanism of claim 1, wherein a device access infrastructure is responsive to a device access call to intercept the call for the selective insertion of faults and the intercept mechanism is operative to return an emulated device response.

11. The test mechanism of claim 1, wherein a device access infrastructure is responsive to a device access call to intercept the call and the intercept mechanism is operable to provide selective insertion of faults prior to effecting the device access.

12. The test mechanism of claim 11, wherein the intercept mechanism operates on data of a device access call with a determined operator and operand.

13. The test mechanism of claim 6, wherein the interface is operable to configure the intercept mechanism for determining when the intercept mechanism injects a fault.

14. The test mechanism of claim 1, wherein the interface comprises an application program interface responsive to a test application for determining a test pattern.

15. A test application on a carrier medium for a test mechanism according to claim 14, the test application comprising computer code configured to be operable:

to provide the interface with a test configuration;

to detect the response of a device driver to a test condition inserted by the intercept mechanism;

to compare the detected response to an expected response set out in a test script;

and

to identify discrepancies between the detected response and the expected response.

16. The test application of claim 15, wherein the test application comprises computer code configured to be operable to maintain a log of the detected responses.

17. A computer program product on a carrier medium, the computer program product comprising an intercept mechanism for intercepting device access calls from a device driver under test and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined desired test pattern.

18. A test mechanism for testing device driver hardening, the test mechanism comprising a means for intercepting device driver access calls from a device driver under test and means for injecting a fault in a response to the device access call according to a determined test pattern.

19. A computer comprising a device driver for accessing an I/O device and a test mechanism for testing device driver hardening, the test mechanism comprising an intercept mechanism for intercepting device access calls from a device driver under test and an interface for configuring the intercept mechanism for faults to be injected in response to the device access calls according to a determined test pattern.

20. A method of testing the hardening of a device driver, the method comprising intercepting device driver access calls from the device driver and injecting a fault in a device driver access according to a desired test pattern.

21. The method of claim 20, comprising a mapping the device access call to at least one intercept routine for handling the device access call.

22. The method of claim 21, comprising mapping a device access call to an intercept routine according to a device access call type.

23. The method of claim 20, comprising monitoring device access call to determine when to inject a fault.

24. The method of claim 23, comprising modifying a count for each device access call of a given type and injecting a fault in response to predetermined count being attained.

25. The method of claim 24, comprising separately monitoring each type of call.

26. The method of claim 24, comprising a further step of monitoring a number of times the fault is to be injected in sequence.